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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/566,554	01/27/2006	Christian Hentschel	NL030941	7342

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EXAMINER	
SHAH, TUSHAR S	
ART UNIT	**PAPER NUMBER**
2184	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/566,554	HENTSCHEL ET AL.	
	Examiner	Art Unit	
	Tushar S. Shah	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/27/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the application filed on 1/27/2006.

Status of Claims

Claims 1-10 have been presented for examination. Claims 1 and 9 are in independent form. Claims 1-10 are rejected under U.S.C. 103(a).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tetrick, US Patent No. 5,737,615 (Hereinafter Tetrick) in view of Benzschawel et al, US Patent No. 5,388,217 (Hereinafter Benzschawel).

Referring to claim 1, Tetrick discloses, a plurality of processing elements (COP1, COP2) (CPU's 1 to N, Tetrick column 3, lines 28-30 and Fig. 1), which are

arranged for synchronously processing data under control of at least one clock facility (each processor has an internal clock, Tetrick, column 3, lines 64).

Also, Tetrick discloses, at least one local controller (CTR1, CTR2) (power down control register 128 and the advanced programmable interrupt controller (APIC), Tetrick column 4, lines 23-25 and column 3, lines 33-36) associated with a processing element of the plurality of processing elements;

Additionally, Tetrick discloses, a data communication means (SB) (multiprocessor bus 118, Tetrick, column 3, lines 35-37) arranged for exchanging data between processing elements of the plurality of processing elements, wherein the local controller is arranged for powering down its associated processing element (the power down input is used to power down or put to sleep a processor, Tetrick columns 3-4, lines 67 and 1-2).

However Tetrick does not disclose, depending on the required processing capacity of that processing element, as recited in the instant claim.

On the other hand, Benzschawel achieves the claimed feature, depending on the required processing capacity of that processing element (The CPU's in the CPU cluster have queues of parameter packets, which to manage their I/O services, and as these parameter packets are processed, interrupts are set for the processor, Benzschawel column 11, lines 33-34, 40-42 and 58-61).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Tetrick to power down CPUs based on the completion of parameter packets in the parameter packet queue of Benzschawel. Tetrick utilizes

interrupts in tandem with the PDI register to control the online/offline state of the CPU's. Benzschawel states that it produces appropriate interrupts based on the completion of the packages. Therefore it clearly follows from this that when the parameter packet queue of Benzschawel is emptied, a flag to place the CPU to sleep or offline may be set. The motivation to combine is apparent in Tetrick, as the suggestion that CPU's that are inactive should be powered down (Tetrick, column 4, lines 9-11).

As per claim 2, most of the limitations of the claim have been met in the rejection of claim 1. See the rejection of claim 1 for details.

Tetrick further discloses, a data processing system according to claim 1, wherein the local controller is further arranged for powering up its associated processing element depending on the required processing capacity of that processing element (while the CPU has been taken offline, it maybe reactivated by the PDI control register or by a interrupt request by another processor, Tetrick column 4, lines 31-33 and 36-39).

As per claim 3, most of the limitations of the claim have been met in the rejection of claim 1. See the rejection of claim 1 for details.

Tetrick does not disclose, a data processing system according to claim 1, further comprising: at least one buffer (B11, B12) associated with the processing element of the plurality of processing elements, wherein the buffer is arranged for exchanging data between its associated processing element and the data communication means, and

wherein the local controller is arranged to determine the required processing capacity of its associated processing element from the filling degree of the associated buffer.

On the other hand, Benzschawel achieves the claimed feature, a data processing system according to claim 1, further comprising: at least one buffer (B11, B12) (the control processor reads the current parameter packet to determine the main memory access o the parameter packet in its work queue, Benschawel column 11, lines 48-50) associated with the processing element of the plurality of processing elements, wherein the buffer is arranged for exchanging data between its associated processing element and the data communication means (the parameter packet is stored in dedicated memory the channel adaptor/arbitrator couples the CPU to external devices via serial channel Benzschawel, Fig 2), and wherein the local controller is arranged to determine the required processing capacity of its associated processing element from the filling degree of the associated buffer (the parameter packet queue provides the I/O kernel information on the packets have been issued and which have been completed and can redirect packets if that particular processor is unable to process the packet, Benzschawel, columns 11-12, lines 66-67 and 1-2).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system and method of Tetrick to include the parameter packet queue of Benzschawel. The motivation to combine is apparent in that the parameter packet queue gives the system of Tetrick a metric to determine when to activate or deactivate processors in the system in order to achieve the stated goal of Tetrick, which is to save power by powering down inactive components of a computer system.

As per claim 4, most of the limitations of the claim have been met in the rejection of claim 1. See the rejection of claim 1 for details.

Tetrick does not disclose, a data processing system according to claim 1, further comprising a control processor, wherein the local controller is arranged to receive information on the required processing capacity of the associated processing element from the control processor, and wherein the local controller is further arranged to have information on the processing capacity of the associated processing element.

On the other hand, Benzschawel discloses, a data processing system according to claim 1, further comprising a control processor (Control processor, Benzschawel column 11, lines 48-50) wherein the local controller is arranged to receive information on the required processing capacity of the associated processing element from the control processor, and wherein the local controller is further arranged to have information on the processing capacity of the associated processing element (the parameter packet queue provides the I/O kernel information on the packets have been issued and which have been completed and can redirect packets if that particular processor is unable to process the packet, Benzschawel, columns 11-12, lines 66-67 and 1-2).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system and method of Tetrick to include the parameter packet queue of Benzschawel and utilize it to mange the flow of packets. The motivation to combine is apparent in that the parameter packet queue gives the system of Tetrick a

metric to determine when to activate or deactivate processors in the system in order to achieve the stated goal of Tetrick, which is to save power by powering down inactive components of a computer system.

As per claim 5, most of the limitations of the claim have been met in the rejection of claim 1. See the rejection of claim 1 for details.

Tetrick does not disclose, a data processing system according to claim 1, wherein the processing element of the plurality of processing elements is further arranged to generate an interrupt for notifying its associated local controller on the required processing capacity.

On the other hand, Benzschawel achieves the claimed feature of, a data processing system according to claim 1, wherein the processing element of the plurality of processing elements is further arranged to generate an interrupt for notifying its associated local controller on the required processing capacity (as each parameter packet is processed appropriate interrupt flags are generated as are needed resulting from the processing, Benzschawel column 11, lines 58-61).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system and method of Tetrick to include the parameter packet queue of Benzschawel and utilize it to mange the flow of packets. The motivation to combine is apparent in that the parameter packet queue gives the system of Tetrick a metric to determine when to activate or deactivate processors in the system in order to

achieve the stated goal of Tetrick, which is to save power by powering down inactive components of a computer system.

As per claim 8, most of the limitations of the claim have been met in the rejection of claim 1. See the rejection of claim 1 for details. Tetrick further discloses, A data processing system according to claim I, further comprising a memory facility (MEM) (Main memory 122, Fig. 1), wherein the data communication means is further arranged for exchanging data between the memory facility and the processing elements of the plurality of processing elements (The main memory device 122 is coupled to the processors by the multiprocessor bus 118, Tetrick column 3, lines 50-52).

Referring to claim 9, claim 1 recites the corresponding limitations as that of claim 9. Therefore, the rejection of claim 1 applies to claim 9.

Note claim 10 recites the corresponding limitations of claim 2. Therefore, the rejection of claim 2 applies to claim 10.

3. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tetrick in view of Benzschawel as applied to claim 1 above, and further in view of Shakkarwar US Publication No. 2004/021598 (hereinafter Shakkarwar).

As per claim 6, most of the limitations of the claim have been met in the rejection of claim 1. See the rejection of claim 1 for details. Tetrick further discloses, A data processing system according to claim 1, wherein a sequence of clock cycles effects a processing operation of an amount of data (the processors have clock circuitry which allows the processor to process the instruction, Tetrick column 4, lines 5-7)

It is noted however that neither Tetrick nor Benzschawel discloses, wherein the data processing system further comprises programmable means for implementing programmable stall clock cycles for the processing element of the plurality of processing elements, wherein the programmable stall clock cycles are interspersed between clock cycles of the sequence of clock cycles, as recited in the instant claim.

On the other hand, Shakkarwar achieves the claimed feature, wherein the data processing system further comprises programmable means for implementing programmable stall clock cycles(Control logic 104 can affect the clock speed and therefore bandwidth of communication between the processors in the system to be suited to the for the processing element of the plurality of processing elements, wherein the programmable stall clock cycles are interspersed between clock cycles of the sequence of clock cycles (a clock may be reduced from 133 MHz to 66MHz in order to save power, Shakkarwar, page 3, lines 1-4).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the methods of Tetrick and Benzschawel in order to have them not only reduce number of processors in the system, but to reduce the data rate between

processors in order to save power. The motivation to combine is apparent in that Shakkarwar's method allows for further reductions in power consumption in a multiprocessor environment, which is the stated goal of Tetrick.

As per claim 7, most of the limitations of the claim have been met in the rejection of claim 1. See the rejection of claim 1 for details.

It is noted that neither Tetrick nor Benzschawel discloses, a data processing system according to claim 1, wherein at least one processing element is associated with a bandwidth control unit (BCTR) for controlling a rate of its data transfer along the data communication means, the bandwidth control unit restricting the data transfer if it exceeds an allowed maximum data rate.

On the other hand, Shakkarwar discloses, as claimed, a data processing system according to claim 1, wherein at least one processing element is associated with a bandwidth control unit (BCTR) (Control logic 104 is used to ensure efficient use of bandwidth, Shakkarwar page 2, paragraph 0023, lines 1-3) for controlling a rate of its data transfer along the data communication means, the bandwidth control unit restricting the data transfer if it exceeds an allowed maximum data rate (the maximum data rate is determined by the amount of data each processor needs to transfer to another processor and its reduced in situations where the excess bandwidth is found. In this manner data rate is reduced when it is found to be greater than the needed maximum bandwidth, Shakkarwar page 2, paragraph 0023, lines 6-11).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the methods of Tetrick and Benzschawel in order to have them not only reduce number of processors in the system, but to reduce the data rate between processors in order to save power. The motivation to combine is apparent in that Shakkarwar's method allows for further reductions in power consumption in a multiprocessor environment, which is the stated goal of Tetrick.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rawson, III US Publication No. 2003/0115495 Published on 6/19/2003 discloses conserving energy in a data processing system by selectively powering down processors.

Kusano US Patent No. 6,745,335 B1 discloses power consumption control of multiprocessor system using separate timers for monitoring processor load rise and drop.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tushar S. Shah whose telephone number is (571)-270-1970. The examiner can normally be reached on Mon-Fri 7:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on 571-272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

T.S.

HENRY TSAI
SUPERVISORY PATENT EXAMINER

12/26/07